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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/713,848

Applicant(s)

GLENN ET AL. *u*

Examiner

David E Graybill

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

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The finality of the Office action mailed 7-18-2 is herein withdrawn, the amendment filed 9-25-2 has been entered, and the claims are further examined on their merits.

The amendment filed 4-25-2 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is the paragraph at page 24, lines 19-24.

Applicant is required to cancel the new matter in the reply to this Office Action.

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 4-15, 20 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Takase (5463229).

At column 1, lines 12-16, column 2, lines 29-32 and 37-43, column 8, lines 51-67, column 9, lines 1-30, column 14, line 66 to column 16, line 5, column 16, lines 43-45, column 17, lines 8-17, column 18, lines 40-64, column 24, lines 34-39, column 28, line 65 to column 29, line 1, column 29, lines 55-59, column 30, lines 10-11 and 34-44, column 30, line 65 to column 31, line 5,

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column 32, lines 32-36, column 33, lines 54-57, column 34, lines 49-51, column 36, lines 24-26, column 37, lines 54-58, and column 38, lines 37-62, Takase teaches the following:

1. A structure comprising: an image sensor 16 having an active area and a bond pad on a first surface of said image sensor; a window 1 having an interior surface and an exterior surface opposite said interior surface; said interior surface of said window facing said first surface of said image sensor, the window having an area of said interior surface that is less than the area of said first surface of said image sensor; the area of said interior surface of said window that is less than the area of said first surface of said image sensor being less than the area of said first surface of said image sensor; and an electrically conductive via 20 extending through said window from said interior surface to said exterior surface of said window, said via being electrically connected to said bond pad.
4. The structure of 1 wherein said active area is responsive to radiation, said window being transparent to said radiation.
5. The structure of 1 further comprising: an electrically conductive interior trace 2 on said interior surface of said window; and an electrically conductive bump 16b electrically connecting said bond pad to said interior trace.

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6. The structure of 5 wherein said interior trace is a land aligned with said via, said bump and said bond pad.

7. The structure of 5 wherein said interior trace is a metallization extending along said interior surface of said window.

8. The structure of 5 wherein said via is offset from said bump, said interior trace extending along said interior surface of said window to electrically connect said via to said bump.

9. The structure of 1 further comprising an electrically conductive exterior trace 3 on said exterior surface of said window, said exterior trace being electrically connected to said via.

10. The structure of 9 further comprising an electrically conductive pad (the portion of the trace connected to the bump 16b) on said exterior trace.

11. The structure of 10 wherein said exterior trace is a land aligned with said via and said pad.

12. The structure of 10 wherein said exterior trace is a metallization extending along said exterior surface of said window.

13. The structure of 10 wherein said via is offset from said electrically conductive pad, said exterior trace extending along

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said exterior surface of said window to electrically connect said via to said electrically conductive pad.

14. The structure of 1 wherein said window includes a central region and a peripheral region, said central region being aligned with said active area, said via being formed within said peripheral region.

15. The structure of 14 further comprising a bead 16b contacting said first surface of said image sensor and further contacting said peripheral region of said window, said bead forming a seal between said peripheral region of said window and said image sensor.

20. The structure of 1 further comprising an image sensor substrate comprising said image sensor.

27. An image sensor package comprising: an image sensor having a bond pad on a first surface of said image sensor; a window having an interior surface; the window having an area of said interior surface that is less than the area of said first surface of said image sensor; the area of said interior surface of said window that is less than the area of said first surface of said image sensor being less than the area of said first surface of said image sensor; an electrically conductive interior trace on said interior surface of said window; and an

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electrically conductive bump electrically connecting said bond pad to said interior trace.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takase as applied to the rejection of claim 1 supra, or in the alternative, the combination of Takase as applied to the rejection of claim 1 supra and Naito (6011320).

Takase does not appear to teach verbatim the following:

3. The structure of 1 wherein said structure is a chip size image sensor package.

Notwithstanding, as cited, Takase teaches that the size of the structure is a result effective variable; namely, that reduced structure size is desirable. Further, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular chip size dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example,

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In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In any case, in the alternative, at column 1, lines 46-54, and column 4, lines 50-51, Naito teaches a chip size package. Furthermore, it would have been obvious to combine the product of Naito with the product of Takase because it would provide a reduced structure size.

Claims 21-23, 26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase as applied to claims 1, 4-15, 20 and 27 supra, and further in combination with Farnworth (5962921).

As cited, Takase teaches the following:

21. An image sensor package comprising: an image sensor having an active area and bond pads on a first surface of said image sensor; a window having an interior surface and mounted to said image sensor, the window having an area of said interior surface that is less than the area of said first surface of said image sensor; the area of said interior surface of said window that is less than the area of said first surface of said image sensor being less than the area of said first surface of said

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image sensor; a plurality of electrically conductive interior traces on an interior surface of said window; a plurality of electrically conductive bumps electrically and physically connecting said bond pads to said interior traces; a plurality of electrically conductive vias extending from said interior surface of said window to an exterior surface of said window, said vias being electrically connected to said interior traces; and a plurality of electrically conductive exterior traces on said exterior surface of said window, said exterior traces being electrically connected to said vias; a plurality of electrically conductive pads on said exterior traces; and a plurality of electrically conductive interconnection bumps on said electrically conductive pads.

22. The image sensor package of 21 wherein said window comprises a central region aligned with said active area and a peripheral region, said interior traces, said vias and said exterior traces being formed within said peripheral region.

23. The image sensor package of 22 further comprising a bead forming a seal between said peripheral region and said image sensor.

26. The image sensor package of 21 further comprising an image sensor substrate comprising said image sensor.

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28. The structure of 10 further comprising an electrically conductive interconnection ball 16b on said electrically conductive pad.

29. An image sensor package comprising: an image sensor having an active area and bond pads on a first surface of said image sensor; a window mounted to said image sensor, the window having an area in a plane parallel to said first surface of said image sensor that is less than the area of said first surface of said image sensor; the area of said window in a plane parallel to said first surface of said image sensor that is less than the area of said first surface of said image sensor being less than the area of said first surface of said image sensor; a plurality of electrically conductive interior traces on an interior surface of said window; a plurality of electrically conductive bumps electrically and physically connecting said bond pads to said interior traces; a plurality of electrically conductive vias extending from said interior surface of said window to an exterior surface of said window, said vias being electrically connected to said interior traces; and a plurality of electrically conductive exterior traces on said exterior surface of said window, said exterior traces being electrically connected to said vias; a plurality of electrically conductive pads on said exterior traces; and a plurality of electrically

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conductive interconnection balls on said electrically conductive pads.

However, Takase does not appear to explicitly teach interconnection balls.

Nevertheless, at column 1, lines 14-44 and column 5, lines 14-22, Farnworth teaches interconnection balls 12A, 12C.

Moreover, it would have been obvious to combine the product of Farnworth with the product of Takase because it would provide interconnection bumps and external connection solder bumps.

Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takase as applied to claim 15 supra, and further in combination with Glenn (5949655).

As cited supra, Takase teaches the following:

16. The structure of 15 wherein said window, said bead, and said image sensor define a cavity.

17. The structure of 16 wherein said active area is responsive to radiation, said cavity containing a medium transparent to said radiation.

18. The structure of 17 wherein said medium is air.

19. The structure of 17 wherein said medium is an encapsulant
10.

However, Takase does not appear to explicitly teach the following:

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16. The structure of 15 wherein said window, said bead, and said image sensor define a sealed cavity.

Nonetheless, at column 1, lines 39-45, column 3, lines 54-60, and column 5, lines 3-18, Glenn teaches wherein a bead 22, and an image sensor 10 define a sealed cavity 19. Moreover, it would have been obvious to combine the invention of Glenn with the invention of Takase because it would provide a protective seal.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Takase and Farnworth as applied to claim 23 supra, and further in combination with Glenn (5949655).

Takase does not appear to explicitly teach the following:
24. The image sensor package of 23 wherein said bead has sides coplanar with sides of said image sensor.

Nonetheless, at column 1, lines 39-45, column 3, lines 54-60, and column 5, lines 3-18, Glenn teaches an image sensor package wherein a bead 22 has sides coplanar with sides of an image sensor 10. Moreover, it would have been obvious to combine the invention of Glenn with the invention of the applied prior art because it would provide a protective seal.

Also, in the combination of the applied prior art, Takase teaches the following:

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25. The image sensor package of 24 wherein said image sensor package is chip size.

To further clarify the teaching wherein the image sensor package is chip size, it is noted that, as cited, Takase teaches a package that includes a bare die along with one or more packaging elements; therefore, as evidenced by the definition of "chip size package" of Farnworth as cited; specifically, "a package that includes a bare die along with one or more packaging elements," Takase teaches wherein the image sensor is chip size.

Applicant's amendment and remarks filed 9-25-2 have been fully considered, and are addressed in the rejection supra and are further addressed infra.

Applicant contends that the term "chip size" is limited in scope to the disclosure of the term in Glenn (6291884), "the resulting BGA, LGA or LCC package is 'chip sized,' i.e., has an area substantially equal to that of the chip itself."

This contention is respectfully traversed because the disclosure of Glenn is not part of the instant original disclosure, and as evidenced by the definitions of the term "chip size" at column 1, lines 21-33 of Glenn (6291884), at column 1, lines 46-54 and column 4, lines 50-51 of Naito (6011310), paragraph [0056] of Harada (2002/0022234), column 1,

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lines 15-19 of Tsuda (6006965), paragraph [0003] of Shoji (2001/0013653), column 1, lines 34-44, column 3, lines 41-44, and column 5, lines 14-31 of Farnworth (5962921), page 3 of Substrate Technology, and page 1 of Value Added Services, the diverse art recognized meanings of the term are not so limited.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.


David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
6-Oct-02